Chapter 5

BJT Biasing Circuits

5.1 The DC Operation Point [5]

DC Bias:

Bias establishes the dc operating point for proper linear operation of an amplifier. If an amplifier is not biased with correct dc voltages on the input and output, it can go into saturation or cutoff when an input signal is applied. Figure 5.1 shows the effects of proper and improper dc biasing of an invert amplifier.

Figure 5.1 Examples of linear and nonlinear operation of an inverting amplifier (the triangle symbol). [5]
In part (a), the output signal is an amplified replica of the input signal except that it is inverted, which means that it is 180° out of the phase with the input. Part (b) illustrates limiting of the positive portion of the output voltage for a result of a dc operating point (Q-point) being too close to cutoff. Part (c) shows limiting of the negative portion of the output voltage as a result of a dc operating point being too close to saturation.

**Linear Operation:**

The region along the load line including all points between saturation and cutoff is generally known as the linear region of the transistor’s operation. The output voltage in this region is ideally a linear reproduction of the input. Figure 5.2 shows an example of the linear operation of a transistor. AC quantities are indicated by lower case italic subscripts.

![Transistor Circuit Diagram](image)

\[ I_{BQ} = \frac{V_{BB} - 0.7V}{R_B} = \frac{3.7V - 0.7V}{10k\Omega} = 300\mu A \]

\[ I_{CQ} = \beta_{DC}I_{BQ} = (100)(300\mu A) = 30 \text{ mA} \]

\[ V_{CEQ} = V_{CC} - I_{CQ}R_C = 10V - (30 \text{ mA})(220 \Omega) = 3.4V \]

Figure 5.2 Variations in collector current and collector-to-emitter voltage as a result of a variation in base current. [5]

Assume a sinusoidal voltage, \( V_{\text{in}} \), is superimposed on \( V_{BB} \), causing the base current to vary sinusoidally 100 \( \mu \text{A} \) above and below its Q-point value of 300 \( \mu \text{A} \). This causes the collector current (\( I_C \)) to vary 10 mA above and below its Q-
point value of 30 mA. As a result, the collector-to-emitter voltage varies 2.2 V above and below its Q-point value of 3.4 V. Point A on the load line corresponds to the positive peak of the sinusoidal input voltage. Point B corresponds to the negative peak, and point Q corresponds to the zero value of the sine wave. $V_{CEQ}$, $I_{CQ}$, and $I_{BQ}$ are dc Q-point values with no input sinusoidal voltage applied.

**Waveform Distortion:**

![Graphical load line illustration of a transistor being driven into saturation and/or cutoff.](image)

Figure 5.3 Graphical load line illustration of a transistor being driven into saturation and/or cutoff. [5]
Under certain input signal conditions, the location of Q-point on the load line can cause one peak of the load line to cause one peak of the $V_{ce}$ waveform to be limited or clipped, as shown in Figure 5.3(a) and (b). In each case, the input signal is too large for the Q-point location and is driving the transistor into cutoff or saturation during a portion of the input cycle. When both peaks are limited, the transistor is being driven into both saturation and cutoff by an excessively large input signal.

Example 1: Determine the Q-point and find the maximum peak value of the base current for linear operation. Assume $\beta_{DC} = 200$.

![Figure 5.4 For Example 1. [5]](image)

Solution:

The Q-point is defined by $I_C$ and $V_{CE}$

$$I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{10V - 0.7V}{47K\Omega} = 198\mu A = I_{BQ}$$

$$I_C = \beta_{DC}I_B = (200)(198\mu A) = 39.6mA = I_{CQ}$$

$$V_{CE} = V_{CC} - I_CR_C = 20V - 13.07 = 6.93V = V_{CEQ}$$
\[ I_{C(sat)} = \frac{V_{CC} - V_{CE(sat)}}{R_C} = I_C(sat) = \frac{V_{CC}}{R_C} = \frac{20V}{330\Omega} \]

\[ I_{Q(cut\,off)} = 0 \]

\[ I_{C(sat)} - I_C = 60.6 - 39.6 = 21mA \]

\[ I_C - I_C(cut\,off) = 39.6 - 0 = 39.6mA \]

\[ \therefore Q\text{-point is in closer to saturation than the cutoff} \]

\[ I_C \text{ is the maximum peak variation (} I_{C(max)} \text{) of the collector current} \]

\[ \therefore I_{b(peak)} = \frac{I_{C(peak)}}{\beta_{DC}} = \frac{21mA}{200} = 105\mu A \]

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**Figure 5.5 For Example 1. [5]**
5.2 Base Bias [5]

As shown in Figure 5.6 (a), two dc voltage supplies are needed to bias a BJT which is not practical. In a simple biasing circuit, $V_{BB}$ is eliminated by connecting the resistor $R_B$ to the supply $V_{CC}$. This biasing circuit is called base bias, or fixed bias, see Figure 5.6 (b).

![Figure 5.6](image)

The analysis of this circuit for the linear region is as follow.

Using KVL:

$$V_{CC} - V_{R_B} - V_{BE} = 0$$

Substituting $I_B R_B$ for $V_{R_B}$

$$V_{CC} - I_E R_B - V_{BE} = 0$$

Then solving for $I_B$,

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$
Kirchhoff’s voltage law applied around the collector circuit gives the following equation:

\[ V_{CC} - I_C R_C - V_{CE} = 0 \]

Solving for \( V_{CE} \),

\[ V_{CE} = V_{CC} - I_C R_C \]

Substituting this expression for \( I_B \) into the formula \( I_C = \beta_{DC} I_B \) yields

\[ I_C = \beta_{DC} \left( \frac{V_{CC} - V_{BE}}{R_B} \right) \]

**Q-Point Stability of Base Bias:**

In the last equation, \( I_C \) is dependent on \( \beta_{DC} \). The disadvantage of this is that \( \beta_{DC} \) varies with temperature and collector current. The variation in \( \beta_{DC} \) causes \( I_C \) and \( V_{CE} \) to change, thus changing the Q-point of the transistor. This makes the base bias circuit extremely beta-dependent and very unstable.

**Example 2:** (a) Determine the Q-point values of \( I_C \) and \( V_{CE} \) for the circuit in Figure 5.7. Assume \( V_{CE} = 8 \text{ V} \), \( R_B = 360 \text{ k}\Omega \) and \( R_C = 2 \text{ k}\Omega \).

(b) Construct the dc load line and plot the Q-point.
Solution:

\[(a) I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{8V - 0.7V}{360K\Omega} = 20.28\mu A\]

\[I_C = \beta_{DC} I_B = 100 \times 20.28\mu A = 2.028mA\]

\[V_{CE} = V_{CC} - I_C R_C = 8V - (2.028mA)(2K\Omega) = 3.94V\]

\[(b) \text{ Assume } V_{CE(sat)} = 0V \therefore I_{C(sat)} = \frac{V_{CC}}{R_C} = \frac{8V}{2K\Omega} = 4mA\]

and \ Assume \ I_{C(cutoff)} = 0.4mA \therefore V_{CE(cutoff)} = V_{CC} = 8V\]

Figure 5.8 For Example 2.
Example 3: Determine the Q-point values of $I_C$ and $V_{CE}$ for the circuit in Figure 5.9. Find $I_{C(sat)}$ and $V_{CE(cut \, off)}$, and then construct the dc load line and plot the Q-point. **Assume $I_C \equiv I_E$ to find $I_{C(sat)}$ and $V_{CE(cut \, off)}$**

![Circuit Diagram](image)

Figure 5.9 For Example 3.

Solution:

Left loop:

\[
V_{CC} - V_{R_B} - V_{BB} - V_{R_E} = 0
\]
\[
V_{CC} - I_B R_1 - V_{BB} - I_E R_E = 0
\]

As $I_E = I_B + I_C = (\beta_{DC} + 1)I_B$

\[
\therefore \quad V_{CC} - I_B R_1 - V_{BB} - 101I_B R_E = 0
\]

\[
I_B = \frac{V_{CC} - V_{BB}}{R_1 + 101R_E} = \frac{20 - 0.7}{2.7 \text{ M}\Omega + 101(3.3 \text{ k}\Omega)}
\]

\[
= 6.363 \mu\text{A}
\]

\[
\therefore \quad I_C = \beta_{DC} I_B = 0.636 \text{ mA}
\]

\[
I_E = I_B + I_C = 0.643 \text{ mA}
\]
Right loop:

\[ V_{CE} - I_C R_C - V_{CE} - I_E R_E = 0 \]

Solving for \( V_{CE} \),

\[ V_{CE} = V_{CC} - I_C R_C - I_E R_E \]

\[ V_{CE} = 20 - (0.636) \times 10 - (0.643) \times 3.3 \]

\[ = 11.52 \, \text{V} \]

\[ \therefore \text{Q-point is at } I_C = 0.636 \, \text{mA and } V_{CE} = 11.52 \, \text{V} \]

\[ V_{CE} = V_C - V_E = (V_{CC} - I_C R_C) - (I_E R_E) \]

\[ I_E \equiv I_C; \quad V_{CE} = V_{CC} - I_C (R_C + R_E) \]

at saturation: \( V_{CE} = 0 \)

\[ \therefore I_{C(set)} = \frac{V_{CC}}{R_C + R_E} = \frac{20V}{(10 + 3.3)K\Omega} = 1.504 \, \text{mA} \]

at cutoff: \( I_{C(cutoff)} = 0A \)

\[ \therefore V_{CE(cutoff)} = V_{CC} = 20V \]

Figure 5.10 For Example 3.
**Example 4:** Determine whether the transistor is biased in cutoff, saturation or linear region.

(a) $R_B = 75K\Omega$, $R_C = 1K\Omega$; saturation

(b) $R_B = 150K\Omega$, $R_C = 1K\Omega$; linear

(c) $R_B = 75K\Omega$, $R_C = 2K\Omega$; saturation

![Figure 5.11 For Example 4. [5]](image)

**Solution:**

\[(a) \text{As} V_{CE} = V_{CC} - I_C R_C\]

\[I_C = \beta_{DC} \left[ \frac{V_{CC} - V_{BE}}{R_B} \right] = 100 \left[ \frac{12 - 0.7}{75K\Omega} \right] = 15.067mA\]

As $I_C > I_{C(sat)} \therefore$ This transistor is biased in saturation region.

\[(b) \text{As} V_{CE} = V_{CC} - I_C R_C\]

\[I_C = \frac{V_{CC}}{R_C} = \frac{12V}{1K\Omega} = 12mA\]
\[ I_C = \beta_{DC} \left( \frac{V_{CC} - V_{BE}}{R_B} \right) = 100 \left[ \frac{12 - 0.7}{150K\Omega} \right] \]

\[ = 7.533mA \]

As \( I_C < I_{C(sat)} \): This transistor is biased in linear region.

\( \left( c \right) \) As \( V_{CE} = V_{CC} - I_C R_C \)

\[ \therefore I_{C(sat)} = \frac{V_{CC}}{R_C} = \frac{12V}{2K\Omega} = 6mA \]

\[ I_C = \beta_{DC} \left( \frac{V_{CC} - V_{BE}}{R_B} \right) = 100 \left[ \frac{12 - 0.7}{75K\Omega} \right] \]

\[ = 7.533mA \]

As \( I_C > I_{C(sat)} \): This transistor is biased in saturation region.

### 5.3 Collector-Feedback Bias [5]

In Figure 5.12, the base resistor \( R_B \) is connected to the collector rather than to \( V_{CC} \). The collector voltage provides the bias for the base-emitter junction. The negative feedback creates an “offsetting” effect that tends to keep the Q-point stable. If \( I_C \) tries to increase, it drops more voltage across \( R_C \), thereby causing \( V_C \) to decrease. When \( V_C \) decreases, there is a decrease in voltage across \( R_B \), which decreases \( I_B \). The decrease in \( I_B \) produces less \( I_C \) which drops less voltage across \( RC \) and thus offsets the decrease in \( V_C \).

![Figure 5.12 Collector-feedback bias. [5]](image_url)
Applying KVL:

\[ V_{CC} = V_{RC} + V_{RB} + V_{BE} \]
\[ = (I_c + I_B)R_c + I_BR_B + V_{BE} \]
\[ = \beta_{DC}I_BR_c + I_BR_B + V_{BE} \]
\[ = (\beta_{DC} + 1)I_BR_c + I_BR_B + V_{BE} \]

\[ I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta_{DC} + 1)R_C} \]

\[ I_{CQ} = \frac{\beta_{DC}(V_{CC} - V_{BE})}{R_B + (\beta_{DC} + 1)R_C} \]

\[ V_{CEQ} = V_{CC} - (I_{CQ} + I_B)R_C \]
\[ \approx V_{CC} - I_{CQ}R_C ; \beta_{DC} >> 1 \]

\[ \therefore V_{CE} \approx V_{CC} - I_cR_C \]

**Q-Point Stability over Temperature:**

It is known that \( \beta_{DC} \) varies directly with temperature, and \( V_{BE} \) varies inversely with temperature. As the temperature goes up in a collector-feedback circuit, \( \beta_{DC} \) goes up and \( V_{BE} \) goes down. This increase in \( \beta_{DC} \) acts to increase \( I_c \). The decrease in \( V_{BE} \) acts to increase \( I_B \) which, in turns also acts to increase \( I_c \). As \( I_c \) tries to increase, the voltage drop across \( R_C \) also tries to increase. This tends to reduce the collector voltage and therefore the voltage across \( R_B \), thus reducing \( I_B \) and offsetting the attempted increase in \( I_c \) and the attempted decrease in \( V_C \). The result is that the collector-feedback circuit maintains a relatively stable Q-point. Moreover, the reverse action occurs when the temperature decreases.
Example 5: Calculate the Q-point values ($I_C$ and $V_{CE}$) for this circuit.

![Image of a transistor circuit](image_url)

Figure 5.13 For Example 5. [5]

Solution:

at Q-point:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta_{DC} + 1)R_C} = \frac{10 - 0.7}{100 + (100 + 1)} = 8.38 \, \mu A$$

$$I_C = \frac{\beta_{DC} (V_{CC} - V_{BE})}{R_B + (\beta_{DC} + 1)R_C} = 100 \times 8.38 \, \mu A = 0.838 \, mA$$

$$V_{CE} = V_{CC} - (I_C + I_B)R_C = 10 - (0.838 + 0.00838) \times 10$$

$$= 1.536 \, V$$

∴ Q-point is at $I_C = 0.838 \, mA$ and $V_{CE} = 1.536 \, V$

at cut off and saturation mode:

As $V_{CE} = V_{CC} - (I_C + I_B)R_C$

But we usually assume that $I_C >> I_B$ to find $I_{C(sat)}$ and $V_{CE(cutoff)}$

Therefore $V_{CE} \approx V_{CC} - I_C R_C$

∴ $I_{C(sat)} = \frac{V_{CC}}{R_C} = 1 \, mA$

$V_{CE(cutoff)} = V_{CC} = 10 \, V$
5.4 Emitter Bias [5]

Emitter bias uses both a positive (+V_{CC}) and a negative (–V_{EE}) supply voltage. In the circuit shown in Figure 5.14, the V_{EE} supply voltage forward-biases the base-emitter junction, Kirchhoff’s voltage law applied around the base-emitter circuit in Figure 5.14 (a), which has been redrawn in Figure 5.14 (b) for analysis, gives the follow equation:

\[- V_{EE} + V_{R_B} + V_{BE} + V_{R_E} = 0\]

Using Ohm’s law,

\[- V_{EE} + I_B R_B + V_{BE} + I_E R_E = 0\]

Solving for V_{EE},

\[I_B R_B + V_{BE} + I_E R_E = V_{EE}\]

Substituting for I_E,

\[I_B R_B + V_{BE} + (\beta_{DC} + 1)I_B R_E = V_{EE}\]

Then solving for I_B,

\[I_B = \frac{V_{EE} - V_{BE}}{R_E + (\beta_{DC} + 1)R_E}, \quad \text{Since } I_C = \beta_{DC} I_B, \quad I_C = \frac{\beta_{DC} (V_{EE} - V_{BE})}{R_E + (\beta_{DC} + 1)R_E}\]

The emitter voltage with respect to ground is

\[V_E = -V_{EE} + I_E R_E\]

The base voltage with respect to ground is

\[V_B = V_E + V_{BE}\]

The collector voltage with respect to ground is

\[V_C = V_{CC} - I_C R_C\]

\[\therefore V_{CE} = V_C - V_E = (V_{CC} - I_C R_C) - (V_{EE} + I_E R_E) = V_{CC} + V_{EE} - I_C R_C - I_E R_E\]

\[\approx (V_{CC} + V_{EE}) - I_C (R_C + R_E), \quad \text{if } \beta_{DC} \gg 1\]
Q-Point Stability of Emitter Bias:

The formula for $I_E$ shows that the emitter bias circuit is dependent on $V_{BE}$ and $\beta_{DC}$, both of which change with temperature and current

$$I_C = \frac{\beta_{DC}(V_{EE} - V_{BE})}{R_B + (\beta_{DC} + 1)R_E} = \frac{V_{EE} - V_{BE}}{\beta_{DC}}$$

If $\beta_{DC} >> 1$, $I_C \approx \frac{V_{EE} - V_{BE}}{R_B + R_E}$

This condition makes $I_C$ independent of $\beta_{DC}$

If $V_{EE} >> V_{BE}$, the $V_{BE}$ term can be dropped, $I_C \equiv \frac{V_{EE}}{R_E}$

This condition makes $I_C$ independent of $V_{BE}$

As $I_C$ is independent of $\beta_{DC}$ and $V_{BE}$, emitter bias can provide a stable Q-point if properly designed.
Example 6: Determine whether the transistor is biased in cutoff, saturation or linear region.

(a) $R_B = 330\Omega$, $R_E = 3K\Omega$, $R_C = 1.6K\Omega$
(b) $R_B = 150\Omega$, $R_E = 1K\Omega$, $R_C = 1.6K\Omega$
(c) $R_B = 150\Omega$, $R_E = 500\Omega$, $R_C = 4\; K\Omega$

\[ \beta_{DC} = 220 \]

\[ +25\; V \]

\[ -5\; V \]

Figure 5.15 For Example 6.

Solution:

(a) As $I_C = \frac{\beta_{DC}(V_{EE} - V_{BE})}{R_B + (\beta_{DC} + 1)R_E}$

\[ \therefore I_{CQ} = \frac{220(5 - 0.7)}{330\Omega + (220 + 1) \times 3\; k\Omega} = 1.426\; mA \]

from $V_{CE} \approx (V_{CC} + V_{EE}) - I_C(R_C + R_E)$, $\beta_{DC} >> 1$

\[ \therefore I_{C(sat)} = \frac{V_{CC} + V_{EE}}{R_C + R_E} = \frac{5 + 25}{3 + 1.6} = 6.522\; mA \]

As $I_{CQ} < I_{C(sat)}$, $\therefore$ this transistor is operated in active mode.

(b) As $I_C = \frac{\beta_{DC}(V_{EE} - V_{BE})}{R_B + (\beta_{DC} + 1)R_E}$
\[ I_{CQ} = \frac{220(5 - 0.7)}{150 \Omega + (220 + 1) \times 1k\Omega} = 4.278 \text{ mA} \]

from \( V_{CE} \approx (V_{CC} + V_{EE}) - I_{C}(R_{c} + R_{E}) \), \( \beta_{DC} >> 1 \)

\[ I_{C(sat)} = \frac{V_{CC} + V_{EE}}{R_{c} + R_{E}} = \frac{5 + 25}{1 + 1.6} = 11.538 \text{ mA} \]

As \( I_{CQ} < I_{C(sat)} \), \( \therefore \) this transistor is operated in active mode.

\((c)\) As \( I_{C} = \frac{\beta_{DC}(V_{EE} - V_{BE})}{R_{s} + (\beta_{DC} + 1)R_{E}} \)

\[ I_{CQ} = \frac{220(5 - 0.7)}{150 \Omega + (220 + 1) \times 500 \Omega} = 8.55 \text{ mA} \]

from \( V_{CE} \approx (V_{CC} + V_{EE}) - I_{C}(R_{c} + R_{E}) \), \( \beta_{DC} >> 1 \)

\[ I_{C(sat)} = \frac{V_{CC} + V_{EE}}{R_{c} + R_{E}} = \frac{5 + 25}{500 \Omega + 4 \times k\Omega} = 6.67 \text{ mA} \]

As \( I_{CQ} > I_{C(sat)} \), \( \therefore \) this transistor is operated in saturation mode.

**Example 7**: Determine \( I_{C}, V_{CE}, I_{C(sat)} \) and \( V_{CE(cut\ off)} \). Also, construct DC load line and plot Q-point. Assume \( \beta_{DC} = 220 \) and \( I_{E} \approx I_{C} \).
Solution:

As \[ I_C = \frac{\beta_{DC}(V_{EE} - V_{BE})}{R_B + (\beta_{DC} + 1)R_E} \]

\[ \therefore I_{CQ} = \frac{220(15 - 0.7)}{330 \Omega + (220 + 1) \times 3 \times k \Omega} = 4.743 \text{ mA} \]

\[ V_{CE} = V_C - V_E = (V_{CC} - I_C R_C) - (V_{EE} + I_E R_E) \]

Assume \( I_C \approx I_E \),

\[ V_{CE} \approx (V_{CC} + V_{EE}) - I_C (R_C + R_E) \]

\[ = (15 + 15) - 4.743 \text{ mA} (1.6 \text{ k\Omega} + 3 \text{ k\Omega}) \]

\[ = 8.182 \text{ V} \]

\[ V_{CE} \equiv (V_{CC} + V_{EE}) - I_C (R_C + R_E) \]

at saturation mode:

\[ V_{CE_{sat}} = 0 \]

\[ I_{C(sat)} = \frac{V_{CC} + V_{EE}}{R_C + R_E} = \frac{30}{4.6 \text{ k\Omega}} = 6.522 \text{ mA} \]

at cutoff mode:

\[ I_{C(cutoff)} = 0 \]

\[ V_{CE_{cutoff}} = V_{CC} + V_{EE} = 30 \text{ V} \]
5.5 Voltage-Divider Bias [7]

The voltage-divider bias circuit is shown in Figure 5.18. In this figure, $V_{CC}$ is used as the single bias source. A dc bias voltage at the base of the transistor can be developed by a resistive voltage divider consisting of $R_1$ and $R_2$. There are two current paths between point A and ground: one through $R_2$ and the other through the base-emitter junction of the transistor and $R_E$.

![Figure 5.18 Voltage-divider bias. [7]](image)

**Thevenin’s Theorem Applied to Voltage-Divider Bias:**

We can replace the original circuit of voltage-divider bias circuit shown in Figure 5.19 (a) with the thevenin equivalent circuit shown in Figure 5.19 (b). Apply Thevenin’s theorem to the circuit left of point A, with $V_{CC}$ replaced by a short to ground and the transistor disconnected from the circuit. The voltage at point A with respect to ground is

$$V_{TH} = \frac{R_2}{R_1 + R_2} V_{CC}$$

and the resistance is

$$R_{TH} = \frac{R_1}{R_2}$$
Figure 5.19 Thevenizing the bias circuit. [7]

Applying KVL,

\[ V_{TH} - V_{R_{TH}} - V_{BE} - V_{R_E} = 0 \]

Substituting, using Ohm's law, and solving for \( V_{TH} \)

\[ V_{TH} = I_B R_{TH} + V_{BE} + I_E R_E = I_B R_{TH} + V_{BE} + (\beta_{DC} + 1) I_B R_E \]

\[ I_B = \frac{V_{TH} - V_{BE}}{R_{TH} + (\beta_{DC} + 1) R_E}, \quad I_{CQ} = \frac{\beta_{DC} (V_{TH} - V_{BE})}{R_{TH} + (\beta_{DC} + 1) R_E} \]

\[ V_{CEQ} = V_{CC} - I_C R_C - I_E R_E \]

\[ \approx V_{CC} - (R_C + R_E) I_{CQ} ; \quad \beta_{DC} \gg 1 \]

**Stability of Voltage-Divider Bias:**

As \( I_{CQ} = \frac{\beta_{DC} (V_{TH} - V_{BE})}{R_{TH} + (\beta_{DC} + 1) R_E} \)

Here assume \( \beta_{DC} \gg 1 \)

\[ \therefore I_{CQ} \approx \frac{\beta_{DC} (V_{TH} - V_{BE})}{R_{TH} + \beta_{DC} R_E}, \text{ then } I_{CQ} \approx \frac{V_{TH} - V_{BE}}{\beta_{DC} + R_E} \]
If \( R_E \gg R_{TH}/\beta_{DC} \), then \( I_C \approx \frac{V_{TH} - V_{BE}}{R_E} \).

This last equation shows that \( I_C \) is independent of \( \beta_{DC} \). Therefore, the voltage-divider bias is widely used because reasonably good stability is achieved with a single supply voltage.

**Example 8:** Determine \( V_{CE} \) and \( I_C \) in the voltage-divider biased transistor circuit. Assume \( \beta_{DC} = 100 \) and \( I_E \approx I_C \).

![Figure 5.20 For Example 8. [7]](image)

**Solution:**

\[
V_{TH} = \frac{R_2}{R_1 + R_2} \frac{V_{CC}}{10 + 5.6} \times 10 = 3.59 \text{ V}
\]

\[
R_{TH} = R_1/R_2 = 5.6/10 = 3.59 \text{ k\Omega}
\]
Example 9: Determine $V_{CE}$ and $I_C$ in the voltage-divider biased transistor circuit. Assume $\beta_{DC} = 50$ and $I_E = I_B + I_C$.

Solution:

\[
I_B = \frac{V_{TH} - V_{BE}}{R_{TH} + (\beta_{DC} + 1)R_E} = \frac{3.59 - 0.7}{3.59 \text{k}\Omega + (100 + 1)560 \text{\Omega}} = 48.046 \mu\text{A}
\]

\[
I_{CQ} = \frac{\beta_{DC}(V_{TH} - V_{BE})}{R_{TH} + (\beta_{DC} + 1)R_E} = 100 \times 48.046 \mu\text{A} = 4.805 \text{mA}
\]

\[
V_{CEQ} \approx V_{CC} - (R_C + R_E)I_{CQ}
\]

\[
\approx 10 - (1 \text{k}\Omega + 560 \text{\Omega}) \times 4.805 \text{mA} = 2.504 \text{V}
\]

Figure 5.21 For Example 9.
Example 10: Determine Q-point \((I_C, V_{CE})\), \(I_{RC}\) and \(I_{RL}\). Assume \(\beta_{DC} = 200\) and \(I_E \equiv I_C\).

\[
I_C = \frac{\beta_{DC}(V_{TH} - V_{BE})}{R_{TH} + (\beta_{DC}+1)R_E} = 50 \times 35.935 \mu A
\]
\[
= 1.797 \text{mA}
\]

Here \(I_E = I_B + I_C = 1.797 \text{mA} + 35.935 \mu A\)
\[\therefore I_E = 1.833 \text{mA}\]

\[
V_{CE} = V_{CC} - I_C R_C - I_E R_E
\]
\[
= 20 - 1.797 \times 1 - 1.833 \times 1
\]
\[
= 16.37 \text{V}
\]

Solution:

\[
V_{TE} = \frac{R_2}{R_1 + R_2} \times V_{CC} = \frac{5}{5 + 5} \times 20 = 10 \text{ V}
\]

\[
R_{TH} = \frac{R_1}{R_2} = 5/5 = 2.5 \text{ k}\Omega
\]
\[ I_B = \frac{V_{TH} - V_{BE}}{R_{TH} + (\beta_{DC} + 1)R_E} = \frac{10 - 0.7}{2.5 \, \text{k}\Omega + (200 + 1)2 \, \text{k}\Omega} = 22.99 \, \mu\text{A} \]

\[ I_{CQ} = \frac{\beta_{DC}(V_{TH} - V_{BE})}{R_{TH} + (\beta_{DC} + 1)R_E} = 200 \times 22.99 \, \mu\text{A} = 4.598 \, \text{mA} \approx I_E \]

Figure 5.23 For Example 10.

\[ I_{R_c} = I_C + I_{R_L} \]

\[ \frac{20 - V_C}{1 \, \text{k}\Omega} = 4.598 + \frac{V_C}{R_L} \]

\[ V_C = 10.268 \, \text{V} \]

\[ V_E = I_E R_E \approx 4.598 \times 2 \, \text{k}\Omega = 9.196 \, \text{V} \]

\[ V_{CE} = V_C - V_E = 1.072 \, \text{V} \]

\[ I_{R_c} = \frac{20 - 10.268}{1 \, \text{k}\Omega} = 9.732 \, \text{mA} \]

\[ I_{R_L} = \frac{10.268}{2 \, \text{k}\Omega} = 5.134 \, \text{mA} \]
**Practice Problem 1:** Determine $I_E$, $I_B$, $I_C$, $\beta_{DC}$, $\alpha_{DC}$ and $V_{EC}$ in the circuit.

![Circuit Diagram]

Figure 5.24 For Practice Problem 1.
Practice Problem 2: Assume $\beta_{DC} = 150$, $V_{CE(sat)} = 0$ V and $I_{C(cut\ off)} = 0$ A.

(a) Let $V_{BB} = 10$ V, determine the Q-point value of $I_C$ and $V_{CE}$.

(b) If $I_C/I_B = 5$, find $V_{BB}$ such that $I_C/I_B = 5$. And determine $I_B$, $I_C$ and $I_E$.

Figure 5.25 For Practice Problem 2.
5.6 Homework 8
1. Determine the Q-point and construct dc load line for this transistor.

![Transistor Circuit](image)

Figure 5.26 For problem 1. [7]

2. Assume $\beta_{dc} = 100$ and $I_E \approx I_C$.
   
   (a) Find $V_E$, $V_C$  
   (b) Determine Q-point of this transistor  
   (c) Construct DC load line and plot Q-point  
   (d) Calculate $I_C$ if $R_B$ is changed from 10 k$\Omega$ to be 1 k$\Omega$

![Transistor Circuit](image)

Figure 5.27 For problem 2.
3. Find the values of $I_B$, $I_C$, $I_E$ and $V_{CE}$. Assume $\beta_{DC} = 100$, and $I_E = I_B + I_C$.

![Figure 5.28 For problem 3.](image)

4. For the circuit shown in this figure, the Q-point is at $I_C = 1$ mA and $V_{CE} = 24$ V when $\beta_{DC} = 60$. Assume $I_C \approx I_E$, $V_{CE(sat)} = 0$ V and $I_{C(cut \ off)} = 0$ A.

(a) Determine the values of $R_C$ and $R_B$.

(b) Construct the DC load line and plot the Q-point.

![Figure 5.29 For problem 4.](image)
5. (a) Determine the Q-point.

(b) Find the maximum peak value of base current for linear operation. Assume $\beta_{DC} = 220$.

![Transistor Circuit](image)

Figure 5.30 For problem 5.

6. (a) Determine the DC operating point (Q-point) and construct the DC load line for the transistor in Figure 6. Assume $I_C \equiv I_E$, $V_{CE(sat)} = 0$ V and $\beta_{DC} = \beta_{ec} = 150$.

(b) Suppose an AC voltage source ($V_{in}$) is connected to the base terminal of the transistor to make $I_b = 100 \ \mu A_F$. Draw the waveform of the total collector current $i_c$ (DC current + AC current i.e., $I_c + I_{c'})$ and that of the total voltage at collector with respect to emitter $v_{ce}$ (DC voltage + AC voltage i.e., $V_{ce} + V_{ce'}$). Also determine the minimum and maximum values of both waveforms.
7. Consider the circuit shown in Figure 5.32. Assume $\beta_{DC} = 100$, $V_{CE(sat)} = 0$ V and $I_{C(cut\ off)} = 0$ A.

(a) Determine the value of $R_B$ to make $I_B = 50 \mu$A, and then find $V_{CE}$ in the circuit.

(b) Determine the value of $R_B$ to make $I_C/I_B = 10$. 

Figure 5.32 For problem 7.
8. (a) Determine the Q-point and construct the DC load line for the transistor in this circuit. Assume $V_{CE(sat)} = 0$ V, $I_{C(cut\,off)} = 0$ mA, $I_C \approx I_E$ and $\beta_{DC} = \beta_{ac} = 150$.

(b) Suppose an AC voltage source ($V_{in}$) is connected to the base terminal of the transistor to make $I_{b(peak)} = 5$ $\mu$A. Draw the waveform of the total collector current $i_c$ (DC current + AC current i.e., $I_C + I_i$) and that of the total voltage at collector with respect to emitter $v_{ce}$ (DC voltage + AC voltage i.e., $V_{CE} + V_{ce}$). Also determine the minimum and maximum values of both waveforms.

\[
\beta_{DC} = \beta_{ac} = 150 \quad \quad + V_{CC} \\
\quad \quad + 15 \, V \\
R_E = 10 \, k\Omega \\
R_C = 10 \, k\Omega \\
R_B = 2 \, M\Omega \\
+ V_{EE} \\
- 30 \, V
\]

Figure 5.33 For problem 8.
9. (a) Consider the circuit in Figure 5.34 (a) and then find $R_{TH}$ and $V_{TH}$ for the base terminal as shown in Figure 5.34 (b).

(b) Find the values of $I_B$, $I_C$ and $I_{RL}$ in the circuit of Figure 4(b). Assume $\beta_{DC} = 100$.

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![Circuit Diagram](image)

Figure 5.34 For problem 9.
10. Consider the circuit shown in Figure 5.35. Assume $\beta_{DC} = 50$, $V_{CE(sat)} = 0$ V and $I_{C(cut\ off)} = 0$ A.

   (a) Let $V_{BB} = 15$ V, determine the Q-point value of $I_C$ and $V_{CE}$ in the circuit.

   (b) Determine the value of $V_{BB}$ to make $I_C/I_B = 10$, and then calculate $I_B$, $I_C$ and $I_E$.

Figure 5.35 For problem 10.