Lecture #3
BJT Biasing Circuits

Instructor:
Dr. Ahmad El-Banna
Agenda

1. Operating Point
2. Transistor DC Bias Configurations
3. Design Operations
4. Various BJT Circuits
5. Troubleshooting Techniques & Bias Stabilization
6. Practical Applications
Introduction

- Any increase in ac voltage, current, or power is the result of a transfer of energy from the applied dc supplies.
- The analysis or design of any electronic amplifier therefore has two components: a dc and an ac portion.

- Basic Relationships/formulas for a transistor:

\[ V_{BE} \approx 0.7 \text{ V} \]

\[ I_E = (\beta + 1)I_B \approx I_C \]

\[ I_C = \beta I_B \]

- **Biasing** means applying of dc voltages to establish a fixed level of current and voltage. >>> Q-Point
Operating Point

- For transistor amplifiers the resulting dc current and voltage establish an operating point on the characteristics that define the region that will be employed for amplification of the applied signal.
- Because the operating point is a fixed point on the characteristics, it is also called the quiescent point (abbreviated Q-point).

Transistor Regions Operation:
1. Linear-region operation:
   - Base–emitter junction forward-biased
   - Base–collector junction reverse-biased
2. Cutoff-region operation:
   - Base–emitter junction reverse-biased
   - Base–collector junction reverse-biased
3. Saturation-region operation:
   - Base–emitter junction forward-biased
   - Base–collector junction forward-biased
TRANSISTOR DC BIAS CONFIGURATIONS

- Fixed-Bias Configuration
- Emitter-Bias Configuration
- Voltage-Divider Bias Configuration
- Collector Feedback Configuration
- Emitter-Follower Configuration
- Common-Base Configuration
- Miscellaneous Bias Configurations
Fixed-Bias Configuration

- Fixed-bias circuit.
- DC equivalent ct.

- Base–emitter loop.
- Collector–emitter loop.

\[ +V_{CC} - I_B R_B - V_{BE} = 0 \]

\[ I_B = \frac{V_{CC} - V_{BE}}{R_B} \]

\[ V_{CE} = V_C \]

\[ V_{CE} = V_{CC} - I_C R_C \]

\[ V_{BE} = V_B - V_E \]
**Fixed-Bias Configuration Example**

**EXAMPLE 4.1** Determine the following for the fixed-bias configuration

a. $I_{BQ}$ and $I_{CQ}$

b. $V_{CEq}$

c. $V_B$ and $V_C$

d. $V_{BC}$

**Solution:**

a. Eq. (4.4): $I_{BQ} = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12 \text{ V} - 0.7 \text{ V}}{240 \text{ k}\Omega} = 47.08 \mu\text{A}$

Eq. (4.5): $I_{CQ} = \beta I_{BQ} = (50)(47.08 \mu\text{A}) = 2.35 \text{ mA}$

b. Eq. (4.6): $V_{CEq} = V_{CC} - I_C R_C$

$= 12 \text{ V} - (2.35 \text{ mA})(2.2 \text{ k}\Omega)$

$= 6.83 \text{ V}$

c. $V_B = V_{BE} = 0.7 \text{ V}$

$V_C = V_{CE} = 6.83 \text{ V}$

d. Using double-subscript notation yields

$V_{BC} = V_B - V_C = 0.7 \text{ V} - 6.83 \text{ V}$

$= -6.13 \text{ V}$

with the negative sign revealing that the junction is reversed-biased, as it should be for linear amplification.
Fixed-Bias Configuration ...

- **Transistor Saturation**

- Saturation regions:
  (a) Actual
  (b) approximate.

- Determining $I_{C_{sat}}$

- Determining $I_{C_{sat}}$ for the fixed-bias configuration.

\[
R_{CE} = \frac{V_{CE}}{I_C} = \frac{0 \text{ V}}{I_{C_{sat}}} = 0 \text{ } \Omega
\]

\[
I_{C_{sat}} = \frac{V_{CC}}{R_C}
\]
Fixed-Bias Configuration ...

- Load Line Analysis

\[ V_{CE} = V_{CC} - I_c R_C \]

\[ V_{CE} = V_{CC} - (0) R_C \]

\[ V_{CE} = V_{CC} \mid I_c=0 \text{ mA} \]

\[ 0 = V_{CC} - I_c R_C \]

\[ I_C = \frac{V_{CC}}{R_C} \mid V_{CE}=0 \text{ V} \]

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**Load-line analysis:** (a) the network; (b) the device characteristics.

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**FIG. 4.13**

Movement of the Q-point with increasing level of \( I_B \)

**FIG. 4.14**

Effect of an increasing level of \( R_C \) on the load line and the Q-point.

**FIG. 4.15**

Effect of lower values of \( V_{CC} \) on the load line and the Q-point.
Emitter-Bias Configuration

- BJT bias circuit with emitter resistor.
- DC equivalent circuit

**Base-Emitter Loop**

\[ +V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0 \]

\[ I_E = (\beta + 1)I_B \]

\[ I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} \]

\[ R_I = (\beta + 1)R_E \]
Emotion-Bias Configuration

Collector-Emitter Loop

\[ +I_{RE} + V_{CE} + I_C R_C - V_{CC} = 0 \]

\[ I_E \equiv I_C \]

\[ V_{CE} = V_{CC} - I_C (R_C + R_E) \]

\[ V_E = I_E R_E \]

\[ V_{CE} = V_C - V_E \]

\[ V_C = V_{CE} + V_E \]

\[ V_B = V_{CC} - I_B R_B \]

\[ V_C = V_{CC} - I_C R_C \]

\[ V_B = V_{BE} + V_E \]

**Example 4.4** For the emitter-bias network of Fig. 4.23, determine:

- a. \( I_B \)
- b. \( I_C \)
- c. \( V_{CE} \)
- d. \( V_C \)
- e. \( V_E \)
- f. \( V_B \)
- g. \( V_{BC} \)

**Solution:**

a. Eq. (4.17):

\[ I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1) R_E} = \frac{20 \text{ V} - 0.7 \text{ V}}{430 \text{ k}\Omega + (51)(1 \text{ k}\Omega)} \]

\[ = \frac{19.3 \text{ V}}{481 \text{ k}\Omega} = 40.1 \text{ \mu A} \]

b. \( I_C = \beta I_B \)

\[ = (50)(40.1 \text{ \mu A}) \]

\[ \approx 2.01 \text{ mA} \]

c. Eq. (4.19):

\[ V_{CE} = V_{CC} - I_C (R_C + R_E) \]

\[ = 20 \text{ V} - (2.01 \text{ mA})(2 \text{ k}\Omega + 1 \text{ k}\Omega) = 20 \text{ V} - 6.03 \text{ V} \]

\[ = 13.97 \text{ V} \]

d. \( V_C = V_{CC} - I_C R_C \)

\[ = 20 \text{ V} - (2.01 \text{ mA})(2 \text{ k}\Omega) = 20 \text{ V} - 4.02 \text{ V} \]

\[ = 15.98 \text{ V} \]

e. \( V_E = V_C - V_{CE} \)

\[ = 15.98 \text{ V} - 13.97 \text{ V} \]

\[ = 2.01 \text{ V} \]

or

\[ V_E = I_E R_E \approx I_C R_E \]

\[ = (2.01 \text{ mA})(1 \text{ k}\Omega) \]

\[ = 2.01 \text{ V} \]

f. \( V_B = V_{BE} + V_E \)

\[ = 0.7 \text{ V} + 2.01 \text{ V} \]

\[ = 2.71 \text{ V} \]

g. \( V_{BC} = V_B - V_C \)

\[ = 2.71 \text{ V} - 15.98 \text{ V} \]

\[ = -13.27 \text{ V} \text{ (reverse-biased as required)} \]
Emitter-Bias Configuration

- Improved bias stability (check example 4.5)

The addition of the emitter resistor to the dc bias of the BJT provides improved stability, that is, the dc bias currents and voltages remain closer to where they were set by the circuit when outside conditions, such as temperature and transistor beta, change.

- Saturation Level

\[ I_{C_{sat}} = \frac{V_{CC}}{R_C + R_E} \]

- Load Line Analysis

\[ V_{CE} = V_{CC} | I_C = 0 \text{mA} \]

\[ I_C = \frac{V_{CC}}{R_C + R_E} | V_{CE} = 0 \text{V} \]
Voltage-Divider Configuration

- Voltage-divider bias configuration.

- Exact Analysis

DC components of the voltage-divider configuration.

- $R_{Th} = R_1 || R_2$

- $E_{Th} = V_{R_2} = \frac{R_2 V_{CC}}{R_1 + R_2}$

- $I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E}$

- $V_{CE} = V_{CC} - I_C (R_C + R_E)$
Voltage-Divider Configuration

- **Approximate Analysis**

  - **Transistor Saturation**

    \[
    I_{C_{\text{sat}}} = I_{C_{\text{max}}} = \frac{V_{CC}}{R_C + R_E}
    \]

- **Load-Line Analysis**

  - \( I_C = \left. \frac{V_{CC}}{R_C + R_E} \right|_{V_{CE}=0\,V} \)
  
  - \( V_{CE} = V_{CC}\left|_{I_c=0\,mA} \right. \)

\[ V_B = \frac{R_2V_{CC}}{R_1 + R_2} \]

\[ R_i = (\beta + 1)R_E \approx \beta R_E \]

\[ \beta R_E \geq 10R_2 \]

\[ V_E = V_B - V_{BE} \]

\[ V_{CEQ} = V_{CC} - I_C(R_C + R_E) \]
EXAMPLE 4.11 Determine the levels of $I_C$ and $V_{CE}$ for the voltage-divider configuration of Fig. 4.37 using the exact and approximate techniques and compare solutions. In this case, the conditions of Eq. (4.33) will not be satisfied and the results will reveal the difference in solution if the criterion of Eq. (4.33) is ignored.

![Voltage-divider configuration](image)

**Solution:** Exact analysis:

**Eq. (4.33):**

$$\beta R_E \geq 10 R_2$$

$$(50)(1.2 \, \text{k}\Omega) \geq 10(22 \, \text{k}\Omega)$$

$$60 \, \text{k}\Omega \geq 220 \, \text{k}\Omega \text{ (not satisfied)}$$

$$R_{Th} = R_1 R_2 = 82 \, \text{k}\Omega \cdot 22 \, \text{k}\Omega = 17.35 \, \text{k}\Omega$$

$$E_{Th} = \frac{R_2 V_{CC}}{R_1 + R_2} = \frac{22 \, \text{k}\Omega(18 \, \text{V})}{82 \, \text{k}\Omega + 22 \, \text{k}\Omega} = 3.81 \, \text{V}$$

$$I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E} = \frac{3.81 \, \text{V} - 0.7 \, \text{V}}{17.35 \, \text{k}\Omega + (51)(1.2 \, \text{k}\Omega)} = \frac{3.11 \, \text{V}}{78.55 \, \text{k}\Omega} = 39.6 \, \mu\text{A}$$

$$I_C = \beta I_B = (50)(39.6 \, \mu\text{A}) = 1.98 \, \text{mA}$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

$$= 18 \, \text{V} - (1.98 \, \text{mA})(5.6 \, \text{k}\Omega + 1.2 \, \text{k}\Omega)$$

$$= 4.54 \, \text{V}$$

Approximate analysis:

$$V_B = E_{Th} = 3.81 \, \text{V}$$

$$V_E = V_B - V_{RE} = 3.81 \, \text{V} - 0.7 \, \text{V} = 3.11 \, \text{V}$$

$$I_C \approx I_E = \frac{V_E}{R_E} = \frac{3.11 \, \text{V}}{1.2 \, \text{k}\Omega} = 2.59 \, \text{mA}$$

$$V_{CE} \approx V_{CC} - I_C(R_C + R_E)$$

$$= 18 \, \text{V} - (2.59 \, \text{mA})(5.6 \, \text{k}\Omega + 1.2 \, \text{k}\Omega)$$

$$= 3.88 \, \text{V}$$

**Comparing the exact and approximate approaches.**

<table>
<thead>
<tr>
<th></th>
<th>$I_C$ (mA)</th>
<th>$V_{CE}$ (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Exact</td>
<td>1.98</td>
<td>4.54</td>
</tr>
<tr>
<td>Approximate</td>
<td>2.59</td>
<td>3.88</td>
</tr>
</tbody>
</table>

The results reveal the difference between exact and approximate solutions. $I_C$ is about 30% greater with the approximate solution, whereas $V_{CE}$ is about 10% less. The results are notably different in magnitude, but even though $\beta R_E$ is only about three times larger than $R_2$, the results are still relatively close to each other. For the future, however, our analysis will be dictated by Eq. (4.33) to ensure a close similarity between exact and approximate solutions.

$$\beta R_E \geq 10 R_2$$ (4.33)
Collector Feedback Configuration

- DC bias circuit with voltage feedback.

- Base–Emitter Loop

\[ V_{CC} - V_{BE} - \beta I_B (R_C + R_E) - I_B R_F = 0 \]

\[ I_B = \frac{V_{CC} - V_{BE}}{R_F + \beta (R_C + R_E)} \]

\[ R' = R_E. \]

\[ I_C = \frac{\beta V'}{R_F + \beta R'} = \frac{V'}{\frac{R_F}{\beta} + R'} \]

\[ I_{CQ} \approx \frac{V'}{R'} \]

- Collector–Emitter Loop

\[ I_F R_E + V_{CE} + I_C R_C - V_{CC} = 0 \]

Because \( I_C \approx I_C \) and \( I_E \approx I_C \), we have

\[ I_C (R_C + R_E) + V_{CE} - V_{CC} = 0 \]

and

\[ V_{CE} = V_{CC} - I_C (R_C + R_E) \]
Collector Feedback Configuration

- Saturation Conditions

Using the approximation \( I'_C = I_C \)

\[
I_{sat} = I_{C_{max}} = \frac{V_{CC}}{R_C + R_E}
\]

- Load-Line Analysis

Continuing with the approximation \( I'_C = I_C \) results in the same load line defined for the voltage-divider and emitter-biased configurations.

The level of \( I_{BQ} \) is defined by the chosen bias configuration.

**Example 4.14** Determine the dc level of \( I_B \) and \( V_C \) for the network of Fig. 4.42.

**Solution:** In this case, the base resistance for the dc analysis is composed of two resistors with a capacitor connected from their junction to ground. For the dc mode, the capacitor assumes the open-circuit equivalence, and \( R_B = R_{F_1} + R_{F_2} \).

Solving for \( I_B \) gives

\[
I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)} = \frac{18 \text{ V} - 0.7 \text{ V}}{(91 \text{ k}\Omega + 110 \text{ k}\Omega) + (75)(3.3 \text{ k}\Omega + 0.51 \text{ k}\Omega)} = \frac{17.3 \text{ V}}{201 \text{ k}\Omega + 285.75 \text{ k}\Omega} = \frac{17.3 \text{ V}}{486.75 \text{ k}\Omega} = 35.5 \mu\text{A}
\]

\[
I_C = \beta I_B = (75)(35.5 \mu\text{A}) = 2.66 \text{ mA}
\]

\[
V_C = V_{CC} - I_C R_C = V_{CC} - I_C R_C
\]

\[
= 18 \text{ V} - (2.66 \text{ mA})(3.3 \text{ k}\Omega)
\]

\[
= 18 \text{ V} - 8.78 \text{ V}
\]

\[
= 9.22 \text{ V}
\]
Emitter-Follower Configuration

- Common-collector (emitter-follower) configuration.

- dc equivalent ct

\[ i/p \text{ ct} \]

\[-I_B R_B - V_{BE} - I_E R_E + V_{EE} = 0 \]

\[ I_B = \frac{V_{EE} - V_{BE}}{R_B + (\beta + 1)R_E} \]

\[ o/p \text{ ct} \]

\[-V_{CE} - I_E R_E + V_{EE} = 0 \]

\[ V_{CE} = V_{EE} - I_E R_E \]

**EXAMPLE 4.16** Determine \( V_{CEq} \) and \( I_{Eq} \) for the network of Fig. 4.48.

**Solution:**

From Eq. 4.44:

\[ I_B = \frac{V_{EE} - V_{BE}}{R_B + (\beta + 1)R_E} \]

\[ = \frac{20 \text{ V} - 0.7 \text{ V}}{240 \text{ kΩ} + (90 + 1)2 \text{ kΩ}} = \frac{19.3 \text{ V}}{240 \text{ kΩ} + 182 \text{ kΩ}} = 45.73 \mu\text{A} \]

From Eq. 4.45:

\[ V_{CEq} = V_{EE} - I_E R_E \]

\[ = 20 \text{ V} - (90 + 1)(45.73 \mu\text{A})(2 \text{ kΩ}) \]

\[ = 20 \text{ V} - 8.32 \text{ V} \]

\[ = 11.68 \text{ V} \]

\[ I_{Eq} = (\beta + 1)I_B = (91)(45.73 \mu\text{A}) \]

\[ = 4.16 \text{ mA} \]
Common-Base Configuration

- Common-base configuration

\[ -V_{EE} + I_E R_E + V_{BE} = 0 \]
\[ I_E = \frac{V_{EE} - V_{BE}}{R_E} \]
\[ -V_{EE} + I_E R_E + V_{CE} + I_C R_C - V_{CC} = 0 \]
\[ V_{CE} = V_{EE} + V_{CC} - I_E R_E - I_C R_C \]
\[ I_E \equiv I_C \]
\[ V_{CE} = V_{EE} + V_{CC} - I_E (R_C + R_E) \]

- i/p ct

- Determining \( V_{CB} \) & \( V_{CE} \)

\[ V_{CB} + I_C R_C - V_{CC} = 0 \]
\[ V_{CB} = V_{CC} - I_C R_C \]
\[ I_C \equiv I_E \]
\[ V_{CB} = V_{CC} - I_C R_C \]

**EXAMPLE 4.17** Determine the currents \( I_E \) and \( I_B \) and the voltages \( V_{CE} \) and \( V_{CB} \) for the common-base configuration of Fig. 4.52.

![Circuit Diagram](image)

\[ \beta = 60 \]
\[ R_E = 1.2 \, \text{k\Omega} \]
\[ R_C = 2.4 \, \text{k\Omega} \]
\[ V_{EE} = 4 \, \text{V} \]
\[ V_{CC} = 10 \, \text{V} \]

**Solution:** Eq. 4.46:
\[ I_E = \frac{V_{EE} - V_{BE}}{R_E} \]
\[ = \frac{4 \, \text{V} - 0.7 \, \text{V}}{1.2 \, \text{k\Omega}} = 2.75 \, \text{mA} \]
\[ I_B = \frac{I_E}{\beta + 1} = \frac{2.75 \, \text{mA}}{60 + 1} = \frac{2.75 \, \text{mA}}{61} \]
\[ = 45.08 \, \mu\text{A} \]

Eq. 4.47:
\[ V_{CE} = V_{EE} + V_{CC} - I_E (R_C + R_E) \]
\[ = 4 \, \text{V} + 10 \, \text{V} - (2.75 \, \text{mA})(2.4 \, \text{k\Omega} + 1.2 \, \text{k\Omega}) \]
\[ = 14 \, \text{V} - (2.75 \, \text{mA})(3.6 \, \text{k\Omega}) \]
\[ = 14 \, \text{V} - 9.9 \, \text{V} \]
\[ = 4.1 \, \text{V} \]

Eq. 4.48:
\[ V_{CB} = V_{CC} - I_C R_C = V_{CC} - \beta I_B R_C \]
\[ = 10 \, \text{V} - (60)(45.08 \, \mu\text{A})(24 \, \text{k\Omega}) \]
\[ = 10 \, \text{V} - 6.49 \, \text{V} \]
\[ = 3.51 \, \text{V} \]
EXAMPLE 4.18  For the network of Fig. 4.53:

a. Determine $I_C$, and $V_{CEQ}$

b. Find $V_B$, $V_C$, $V_E$, and $V_{BC}$.

Solution:

a. The absence of $R_E$ reduces the reflection of resistive levels to simply that of $R_C$, and the equation for $I_B$ reduces to

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta R_C} = \frac{20 \text{ V} - 0.7 \text{ V}}{680 \text{ k}\Omega + (120)(4.7 \text{ k}\Omega)} = \frac{19.3 \text{ V}}{1.244 \text{ M}\Omega} = 15.51 \mu\text{A}$$

$$I_{CQ} = \beta I_B = (120)(15.51 \mu\text{A}) = 1.86 \text{ mA}$$

$$V_{CEQ} = V_{CC} - I_{CQ} R_C = 20 \text{ V} - (1.86 \text{ mA})(4.7 \text{ k}\Omega) = 11.26 \text{ V}$$

b. 

$$V_B = V_{BE} = 0.7 \text{ V}$$

$$V_C = V_{CE} = 11.26 \text{ V}$$

$$V_E = 0 \text{ V}$$

$$V_{BC} = V_B - V_C = 0.7 \text{ V} - 11.26 \text{ V} = -10.56 \text{ V}$$

EXAMPLE 4.19  Determine $V_C$ and $V_B$ for the network of Fig. 4.54.

Solution:  Applying Kirchhoff’s voltage law in the clockwise direction for the base–emitter loop results in

$$-I_B R_B - V_{BE} + V_{EE} = 0$$

and

Substitution yields

$$I_B = \frac{V_{EE} - V_{BE}}{R_B} = \frac{9 \text{ V} - 0.7 \text{ V}}{100 \text{ k}\Omega} = \frac{8.3 \text{ V}}{100 \text{ k}\Omega} = 83 \mu\text{A}$$

$$I_C = \beta I_B = (45)(83 \mu\text{A}) = 3.735 \text{ mA}$$

$$V_C = -I_C R_C = -(3.735 \text{ mA})(1.2 \text{ k}\Omega) = -4.48 \text{ V}$$

$$V_B = -I_{EB} R_B = -(83 \mu\text{A})(100 \text{ k}\Omega) = -8.3 \text{ V}$$
## Summary Table

**BJT Bias Configurations**

<table>
<thead>
<tr>
<th>Type</th>
<th>Configuration</th>
<th>Pertinent Equations</th>
</tr>
</thead>
</table>
| Fixed-bias            | ![Fixed-bias Circuit](image) | - $I_B = \frac{V_{CC} - V_{BE}}{R_B}$
  - $I_C = \beta I_B$, $I_E = (\beta + 1)I_B$
  - $V_{CE} = V_{CC} - I_C R_C$ |
| Emitter-bias          | ![Emitter-bias Circuit](image) | - $I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}$
  - $I_C = \beta I_B$, $I_E = (\beta + 1)I_B$
  - $R_I = (\beta + 1)R_E$
  - $V_{CE} = V_{CC} - I_C (R_C + R_E)$ |
| Voltage-divider bias | ![Voltage-divider Circuit](image) | EXACT: $R_{Th} = R_1||R_2$, $E_{Th} = \frac{R_2V_{CC}}{R_1 + R_2}$
  - $I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E}$
  - $I_C = \beta I_B$, $I_E = (\beta + 1)I_B$
  - $V_{CE} = V_{CC} - I_C (R_C + R_E)$
  APPROXIMATE: $\beta R_E \geq 10R_2$
  - $V_B = \frac{R_2V_{CC}}{R_1 + R_2}$, $V_C = V_B - V_{BE}$
  - $I_E = \frac{V_E}{R_E}$, $I_B = \frac{I_E}{\beta + 1}$
  - $V_{CE} = V_{CC} - I_C (R_C + R_E)$ |
Summary Table.

**Collector-feedback**

\[ I_B = \frac{V_{CC} - V_{BE}}{R_F + \beta(R_C + R_E)} \]
\[ I_C = \beta I_B, I_E = (\beta + 1)I_B \]
\[ V_{CE} = V_{CC} - I_C(R_C + R_E) \]

**Emitter-follower**

\[ I_B = \frac{V_{EE} - V_{BE}}{R_F + (\beta + 1)R_E} \]
\[ I_C = \beta I_B, I_E = (\beta + 1)I_B \]
\[ V_{CE} = V_{EE} - I_E R_E \]

**Common-base**

\[ I_E = \frac{V_{EE} - V_{BE}}{R_E} \]
\[ I_B = \frac{I_E}{\beta + 1}, I_C = \beta I_B \]
\[ V_{CE} = V_{EE} + V_{CC} - I_E(R_C + R_E) \]
\[ V_{CB} = V_{CC} - I_C R_C \]
DESIGN OPERATION
Design Operations

• Discussions thus far have focused on the analysis of existing networks. All the elements are in place, and it is simply a matter of solving for the current and voltage levels of the configuration.

• The design process is one where a current and/or voltage may be specified and the elements required to establish the designated levels must be determined.

• The design sequence is obviously sensitive to the components that are already specified and the elements to be determined. If the transistor and supplies are specified, the design process will simply determine the required resistors for a particular design.

• Once the theoretical values of the resistors are determined, the nearest standard commercial values are normally chosen and any variations due to not using the exact resistance values are accepted as part of the design.
EXAMPLE 4.21  Given the device characteristics of Fig. 4.59a, determine $V_{CC}$, $R_B$, and $R_C$ for the fixed-bias configuration of Fig. 4.59b.

**Solution:** From the load line

$$V_{CC} = 20 \text{ V}$$

$$I_C = \frac{V_{CC}}{R_C} \bigg|_{V_{CE}=0 \text{ V}}$$

and

$$R_C = \frac{V_{CC}}{I_C} = \frac{20 \text{ V}}{8 \text{ mA}} = 2.5 \text{ k}\Omega$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

with

$$R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{20 \text{ V} - 0.7 \text{ V}}{40 \mu\text{A}} = 19.3 \text{ V} \div 40 \mu\text{A}$$

$$= 482.5 \text{ k}\Omega$$

Standard resistor values are

$$R_C = 2.4 \text{ k}\Omega$$

$$R_B = 470 \text{ k}\Omega$$

Using standard resistor values gives

$$I_B = 41.1 \mu\text{A}$$

which is well within 5% of the value specified.
Design Operations Example..

- Design of a Current-Gain-Stabilized (Beta-Independent) Circuit

**EXAMPLE 4.25** Determine the levels of $R_C$, $R_E$, $R_1$, and $R_2$ for the network of Fig. 4.63 for the operating point indicated.

**Solution:**

Current-gain-stabilized circuit for design considerations.

\[
V_E = \frac{1}{10}V_{CC} = \frac{1}{10}(20 \text{ V}) = 2 \text{ V}
\]

\[
R_E = \frac{V_E}{I_E} = \frac{2 \text{ V}}{10 \text{ mA}} = 200 \text{ k}\Omega
\]

\[
R_C = \frac{V_R}{I_C} = \frac{V_{CC} - V_{CE} - V_E}{10 \text{ mA}} = \frac{20 \text{ V} - 8 \text{ V} - 2 \text{ V}}{10 \text{ mA}} = \frac{10 \text{ V}}{10 \text{ mA}} = 1 \text{ k}\Omega
\]

\[
V_B = V_{BE} + V_E = 0.7 \text{ V} + 2 \text{ V} = 2.7 \text{ V}
\]

\[
R_2 \leq \frac{1}{10}B R_E
\]

and

\[
V_B = \frac{R_2}{R_1 + R_2} V_{CC}
\]

Substitution yields

\[
R_2 \leq \frac{1}{10}(80)(0.2 \text{ k}\Omega)
\]

\[
= 1.6 \text{ k}\Omega
\]

\[
V_B = 2.7 \text{ V} = \frac{(1.6 \text{ k}\Omega)(20 \text{ V})}{R_1 + 1.6 \text{ k}\Omega}
\]

\[
2.7R_1 + 4.32 \text{ k}\Omega = 32 \text{ k}\Omega
\]

\[
2.7R_1 = 27.68 \text{ k}\Omega
\]

\[
R_1 = 10.25 \text{ k}\Omega \quad \text{(use 10 k}\Omega)\]
• MULTIPLE BJT NETWORKS
• CURRENT MIRRORS
• CURRENT SOURCE CIRCUITS
  • Bipolar Transistor Constant-Current Source
  • Transistor/Zener Constant-Current Source
• PNP TRANSISTORS
• TRANSISTOR SWITCHING NETWORKS

VARIOUS BJT CIRCUITS
MULTIPLE BJT NETWORKS

- R–C coupling

- Darlington configuration

\[ \beta_D = \beta_1 \beta_2 \]
\[ I_B = \frac{V_{CC} - V_{BE1} - V_{BE2}}{R_B + (\beta_D + 1)R_E} \]
\[ V_{BE1} = V_{BE} + V_{BE2} \]
\[ V_{CE} = V_{C2} - V_{E2} \]
\[ V_{CE1} = V_{CC} - V_{E2} \]
\[ I_C = I_{E2} = \beta_D I_{B1} \]
MULTIPLE BJT NETWORKS..

- Cascode configuration

\[ I_{R_1} \equiv I_{R_2} \equiv I_{R_3} \gg I_{B_1} \text{ or } I_{B_2} \]

\[ V_{B_1} = \frac{R_3}{R_1 + R_2 + R_3} V_{CC} \]

\[ V_{B_2} = \frac{(R_2 + R_3)}{R_1 + R_2 + R_3} V_{CC} \]

\[ V_{E_1} = V_{B_1} - V_{BE_1} \]

\[ V_{E_2} = V_{B_2} - V_{BE_2} \]

\[ I_{C_1} \equiv I_{E_2} \equiv I_{C_2} \equiv I_{E_1} = \frac{V_{B_1} - V_{BE_1}}{R_{E_1} + R_{E_2}} \]

\[ V_{C_1} = V_{B_2} - V_{BE_2} \]

\[ V_{C_2} = V_{CC} - I_{C_2}R_C \]

\[ I_{R_1} \equiv I_{R_2} \equiv I_{R_3} = \frac{V_{CC}}{R_1 + R_2 + R_3} \]

\[ I_{B_1} = \frac{I_{C_1}}{\beta_1} \quad I_{B_2} = \frac{I_{C_2}}{\beta_2} \]

**FIG. 4.68**
Cascode amplifier.

**FIG. 4.69**
DC equivalent of Fig. 4.68.
MULTIPLE BJT NETWORKS...

- Feedback Pair

\[
\begin{align*}
I_{B_2} &= I_{C_1} = \beta_1 I_{B_1} \\
I_{C_2} &= \beta_2 I_{B_2} \\
I_{C_2} &= I_{E_2} = \beta_1 \beta_2 I_{B_1}
\end{align*}
\]

\[
\begin{align*}
I_C &= I_{E_1} + I_{E_2} \\
&= \beta_1 I_{B_1} + \beta_1 \beta_2 I_{B_1} \\
&= \beta_1 (1 + \beta_2) I_{B_1}
\end{align*}
\]

\[
I_C = \beta_1 \beta_2 I_{B_1}
\]

\[
\begin{align*}
V_{CC} - I_C R_C - V_{EB_1} - I_{B_1} R_B &= 0 \\
V_{CC} - V_{EB_1} - \beta_1 \beta_2 I_{B_1} R_C - I_{B_1} R_B &= 0
\end{align*}
\]

\[
I_{B_1} = \frac{V_{CC} - V_{EB_1}}{R_B + \beta_1 \beta_2 R_C}
\]

FIG. 4.70
Feedback Pair amplifier.

FIG. 4.71
DC equivalent of Fig. 4.70.

\[
\begin{align*}
V_{B_1} &= I_{B_1} R_B \\
V_{C_1} &= V_{CC} - I_C R_C \\
V_{B_2} &= V_{BE_2} \\
V_{C_2} &= V_{CC} - I_C R_C \\
V_{CE_2} &= V_{C_2} \\
V_{EC_1} &= V_{E_1} - V_{C_1} \\
V_{EC_1} &= V_{C_1} - V_{BE_2}
\end{align*}
\]
MULTIPLE BJT NETWORKS....

- Direct Coupled

![Diagram](image)

**FIG. 4.72**
Direct-coupled amplifier.

**FIG. 4.73**
DC equivalent of Fig. 4.72.

\[
I_{B1} = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_{E1}}
\]

\[
R_{Th} = R_1 || R_2
\]

\[
E_{Th} = \frac{R_2V_{CC}}{R_1 + R_2}
\]

\[
V_{B2} = V_{CC} - I_CR_C
\]

\[
V_{E2} = V_{B2} - V_{BE2}
\]

\[
I_{E2} = \frac{V_{E2}}{R_{E2}}
\]

\[
V_{CE2} = V_{C2} - V_{E2}
\]

\[
V_{CE2} = V_{CC} - V_{E2}
\]

- \( R_1 = 33 \text{ k}\Omega \)
- \( R_2 = 10 \text{ k}\Omega \)
- \( R_{E1} = 2.2 \text{ k}\Omega \)
- \( R_{E2} = 1.2 \text{ k}\Omega \)
- \( C_1 = 1 \mu\text{F} \)
- \( C_{E1} = 20 \mu\text{F} \)
- \( V_{CC} = 14 \text{ V} \)
- \( \beta_1 = 100 \)
- \( \beta_2 = 50 \)

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CURRENT MIRRORS

**FIG. 4.74**
Current mirror using back-to-back BJTs.

\[ I_{control} = I_{C_1} + I_B = I_{C_1} + 2I_{B_1} \]
\[ I_{C_1} = \beta_1 I_{B_1} \]
\[ I_{control} = \beta_1 I_{B_1} + 2I_{B_1} = (\beta_1 + 2)I_{B_1} \]

\( \beta_1 \) is typically \( \gg 2 \), \( I_{control} \approx \beta_1 I_{B_1} \).

\[ I_{B_1} = \frac{I_{control}}{\beta_1} \]

**FIG. 4.75**
Base characteristics for transistor \( Q_1 \) (and \( Q_2 \)).

\[ I_L = I_{C_2} = \beta \dot{I}_{B_2} \]

\[ I_{C_2} = \dot{I}_{B_2} \]

**FIG. 4.76**
Current mirror circuit with higher output.

\[ I_{control} = \frac{V_{CC} - 2V_{BE}}{R} \approx \frac{I_C}{\beta} + \frac{1}{\beta} I_C \approx I_C \]

\[ I \approx I_C = I_{control} \]

**FIG. 4.78**
Current mirror connection.

\[ I = I_{DSS} \]
CURRENT SOURCE CIRCUITS

- Bipolar Transistor Constant-Current Source

\[ V_B = \frac{R_1}{R_1 + R_2} (-V_{EE}) \]
\[ V_E = V_B - 0.7 \text{ V} \]
\[ I_E = \frac{V_E - (-V_{EE})}{R_E} \approx I_C \]

**FIG. 4.81**
Discrete constant-current source.

- Transistor/Zener Constant-Current Source

\[ I = I_E = \frac{V_Z - V_{BE (on)}}{R_E} \]

**FIG. 4.83**
Constant-current circuit using Zener diode.
**pnp TRANSISTORS**

**FIG. 4.85**

*pnp transistor in an emitter-stabilized configuration.*

\[-I_E R_E + V_{BE} - I_B R_B + V_{CC} = 0\]

\[I_B = \frac{V_{CC} + V_{BE}}{R_B + (\beta + 1)R_E}\]

\[-I_E R_E + V_{CE} - I_C R_C + V_{CC} = 0\]

\[V_{CE} = -V_{CC} + I_C( R_C + R_E)\]

**FIG. 4.87**

*Transistor inverter.*
TRANSISTOR SWITCHING NETWORKS..

and is depicted in Fig. 4.88.

\[ R_{\text{sat}} = \frac{V_{CE_{\text{sat}}}}{I_{C_{\text{sat}}}} \]

Using a typical average value of \( V_{CE_{\text{sat}}} \) such as 0.15 V gives

\[ R_{\text{sat}} = \frac{0.15 \text{ V}}{6.1 \text{ mA}} = 24.6 \ \Omega \]

\[ R_{\text{cutoff}} = \frac{V_{CC}}{I_{CEO}} = \frac{5 \text{ V}}{0 \text{ mA}} = \infty \ \Omega \]

\[ R_{\text{cutoff}} = \frac{5 \text{ V}}{10 \mu\text{A}} = 500 \ \text{k} \Omega \]

Fig. 4.89: Cutoff conditions and the resulting terminal resistance.

Fig. 4.91: Defining the time intervals of a pulse waveform.

\[ t_{\text{off}} = t_{s} + t_{f} \]
TROUBLESHOOTING TECHNIQUES
TROUBLESHOOTING TECHNIQUES

• For an “on” transistor, the voltage $V_{BE}$ should be in the neighborhood of 0.7 V.
• For the typical transistor amplifier in the active region, $V_{CE}$ is usually about 25% to 75% of $V_{CC}$.

---

**FIG. 4.92**
Checking the dc level of $V_{BE}$

**FIG. 4.93**
Checking the dc level of $V_{CE}$

**FIG. 4.94**
Effect of a poor connection or damaged device.

**FIG. 4.95**
Checking voltage levels with respect to ground.
BIAS STABILIZATION

- The stability of a system is a measure of the sensitivity of a network to variations in its parameters.
- In any amplifier employing a transistor the collector current $I_C$ is sensitive to each of the following parameters:

  - $\beta$: increases with increase in temperature
  - $|V_{BE}|$: decreases about 2.5 mV per degree Celsius ($^\circ$C) increase in temperature
  - $I_{CO}$ (reverse saturation current): doubles in value for every 10$^\circ$C increase in temperature

<table>
<thead>
<tr>
<th>$T$ ($^\circ$C)</th>
<th>$I_{CO}$ (nA)</th>
<th>$\beta$</th>
<th>$V_{BE}$ (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-65</td>
<td>$0.2 \times 10^{-3}$</td>
<td>20</td>
<td>0.85</td>
</tr>
<tr>
<td>25</td>
<td>0.1</td>
<td>50</td>
<td>0.65</td>
</tr>
<tr>
<td>100</td>
<td>20</td>
<td>80</td>
<td>0.48</td>
</tr>
<tr>
<td>175</td>
<td>$3.3 \times 10^{3}$</td>
<td>120</td>
<td>0.3</td>
</tr>
</tbody>
</table>

Stability Factors $S(I_{CO})$, $S(V_{BE})$, and $S(\beta)$

- $S(I_{CO}) = \frac{\Delta I_C}{\Delta I_{CO}}$
- $S(V_{BE}) = \frac{\Delta I_C}{\Delta V_{BE}}$
- $S(\beta) = \frac{\Delta I_C}{\Delta \beta}$

*The higher the stability factor, the more sensitive is the network to variations in that parameter.*
BIAS STABILIZATION \( S(I_{CO}) \)

**Fixed-Bias Configuration**
\[
S(I_{CO}) = \beta
\]

**Emitter-Bias Configuration**
\[
S(I_{CO}) = \frac{\beta(1 + R_B/R_E)}{\beta + R_B/B_E}
\]

**Voltage-Divider Bias Configuration**
\[
S(I_{CO}) = \frac{\beta(1 + R_{Th}/R_E)}{\beta + R_{Th}/R_E}
\]

**Feedback-Bias Configuration \( (R_E = 0 \Omega) \)**
\[
S(I_{CO}) = \frac{\beta(1 + R_B/R_C)}{\beta + R_B/R_C}
\]

**Physical Impact**

- **fixed-bias configuration**
  \[
  I_B = \frac{V_{CC} - V_{BE}}{R_B}
  \]
  a stabilizing effect as described for the emitter-bias configuration.

- **emitter-bias configuration**
  \[
  I_B \downarrow = \frac{V_{CC} - V_{BE} - V_E \uparrow}{R_B}
  \]
  there is a reaction to an increase in \( I_C \) that will tend to oppose the change in bias conditions.

- **feedback configuration**
  \[
  I_B \downarrow = \frac{V_{CC} - V_{BE} - V_{Re} \uparrow}{R_B}
  \]
  the level of \( I_C \) would continue to rise with temperature, with \( I_B \) maintaining a fairly constant value—a very unstable situation.

- **voltage-divider bias**
  \[
  \beta R_E \gg 10R_2
  \]
  The most stable of the configurations
**BIAS STABILIZATION .. \( S(V_{BE}) \& S(\beta) \)**

\[
S(V_{BE}) = \frac{\Delta I_C}{\Delta V_{BE}}
\]

**Fixed-Bias Configuration**

\[
S(V_{BE}) \approx \frac{-\beta}{R_B}
\]

\[
S(\beta) = \frac{I_C}{\beta_1}
\]

**Emitter-Bias Configuration**

\[
S(V_{BE}) \approx \frac{-\beta/R_E}{\beta + R_B/R_E}
\]

\[
\beta \gg R_B/R_E
\]

\[
S(V_{BE}) \approx \frac{-\beta/R_E}{\beta} = \frac{1}{R_E}
\]

**Voltage-Divider Bias Configuration**

\[
S(V_{BE}) = \frac{-\beta/R_E}{\beta + R_{Th}/R_E}
\]

\[
S(\beta) = \frac{I_C(1 + R_B/R_E)}{\beta_1(\beta_2 + R_{Th}/R_E)}
\]

**Feedback-Bias Configuration \((R_E = 0 \Omega)\)**

\[
S(V_{BE}) = \frac{-\beta/R_C}{\beta + R_B/R_C}
\]

\[
S(\beta) = \frac{I_C(R_B + R_C)}{\beta_1(R_B + \beta_2R_C)}
\]

**Summary**

\[
\Delta I_C = S(I_{CO}) \Delta I_{CO} + S(V_{BE}) \Delta V_{BE} + S(\beta) \Delta \beta
\]

**For fixed-bias**

\[
\Delta I_C = \beta \Delta I_{CO} - \frac{\beta}{R_B} \Delta V_{BE} + \frac{I_C}{\beta_1} \Delta \beta
\]

**General Conclusion:**

The ratio \( R_B/R_E \) or \( R_{TV}/R_E \) should be as small as possible with due consideration to all aspects of the design, including the ac response.
• BJT Diode Usage and Protective Capabilities
• Relay Driver
• Light Control
• Maintaining a Fixed Load Current
• Alarm System with a CCS
• Voltage Level Indicator
• Logic Gates

PRACTICAL APPLICATION
Practical Application

- BJT Diode Usage and Protective Capabilities

![Diode Circuit Diagram](image1)

**FIG. 4.102**
BJT applications as a diode: (a) simple series diode circuit; (b) setting a reference level.

- Relay Driver

![Relay Driver Diagram](image2)

**FIG. 4.104**
Relay driver: (a) absence of protective device; (b) with a diode across the relay coil.
Practical Application..

- **Light Control**

  ![Light Control Diagram](image)

  **FIG. 4.105**
  
  Using the transistor as a switch to control the on-off states of a bulb: (a) network; (b) effect of low bulb resistance on collector current; (c) limiting resistor.

- **Maintaining a Fixed Load Current**

  ![Fixed Load Current Diagram](image)

  **FIG. 4.106**
  
  Building a constant-current source assuming ideal BJT characteristics: (a) ideal characteristics; (b) network; (c) demonstrating why $I_C$ remains constant.
Practical Application...

- Alarm System with a CCS

![Diagram of Alarm System]

- Voltage Level Indicator

![Diagram of Voltage Level Indicator]

An alarm system with a constant-current source and an op-amp comparator.

Voltage level indicator.
Practical Application....

• Logic Gates

**FIG. 4.111**

BJT logic gates: (a) OR; (b) AND.
• For more details, refer to:
• The lecture is available online at:
  • [https://speakerdeck.com/ahmad_elbanna](https://speakerdeck.com/ahmad_elbanna)
• For inquires, send to:
  • ahmad.elbanna@fes.bu.edu.eg
  • ahmad.elbanna@ejust.edu.eg